Code No: 134CF

R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year II Semester Examinations, September/October - 2023
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, ECE, MCT)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) Implement OR gate using only two input NAND gates [2]
b) Implement the following Boolean equation using only NAND gates
$Y = AB + CDE + F.$ [3]
c) What is a Full-Subtractor, and write its truth table? [2]
d) What is priority encoder? Mention its operation? [3]
e) What are the different types of shift registers? [2]
f) Give the comparison between Asynchronous and synchronous counters. [3]
g) Differentiate between Moore and Mealy machines in terms of their output characteristics. [2]
h) What is the operation of a serial binary adder? [3]
i) What is state minimization, advantage of using the merger chart method for state minimization? [2]
j) Describe the role of partitioning techniques in the minimization of sequential machines. [3]

PART – B

(50 Marks)

2.a) Simplify the Boolean expression: $F = A + B + \bar{C} + D(E + F)$.
b) Implement the Boolean function using NOR gates. $Y = (A\bar{B} + \bar{A}B)(C + \bar{D})$. [5+5]

OR

3.a) Describe the properties of error-detecting codes and error-correcting codes. How do they enhance the reliability of digital data transmission?
b) Define the concept of duality in Boolean algebra. Provide a pair of dual theorems and explain their relationship. [5+5]

4. Simplify the following Boolean function by using tabulation method and implement by using Universal logic gates. [10]

$$F(A, B, C, D) = \Sigma m(0,1,2,5,6,7,8,9,10,14)$$

OR

5.a) Design and implement a 4-bit Binary-To-Gray code converter.
b) Explain operation Carry Look Ahead Adder with the help of logic diagram. [5+5]

6.a) Design D Flip Flop by using SR Flip Flop and draw the timing diagram.
b) Explain the operation of a universal shift register. [5+5]

OR

7. Design and implement 3-bit ripple counter using J-K flip flop. Draw the state diagram, logic diagram and timing diagram for the same. [10]

8. Design a sequence detector that detects the pattern 11011 using D flip-flops and logic gates. Show the state diagram, state table, flip-flop input equations and logic diagram of the circuit. [10]

OR

9. Design a parity-bit generator circuit for a 7-bit data word. Explain how this parity bit can be used to detect single-bit errors in the received data with an example. [10]

10.a) Create a state diagram for a simple traffic light controller that cycles through the states: Green, Yellow, and Red.
b) Explain the purpose of a state transition table in FSM design. [5+5]

OR

11.a) Describe the merger chart construction and state reduction process for an incompletely specified sequential circuit.
b) With an example, illustrate how states are merged in a merger chart to simplify the sequential circuit? [5+5]

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